



# Synaptic Labs'

## Hyperbus Controller Full Featured Edition Upgrade

### Introduction

This short document outlines the basic steps for upgrading the tutorials in order to use the Full Featured Edition of S/Labs HBMC IP.

### Step 1 Remove HBMC Qsys Component from the project IP Folder or other IP installation location

1. Remove any copy of S/Labs' HBMC basic (open-core) edition IP bundle from your project or IP installation folder.

### Step 2: License Setup

1. Next you need to apply for Synaptic Labs' HyperBus Memory Controller license. You can skip this step if you already installed the license at some earlier stage.

Free enrollment can be obtained from:

[http://opencore\\_license\\_001.synaptic-labs.com/](http://opencore_license_001.synaptic-labs.com/)

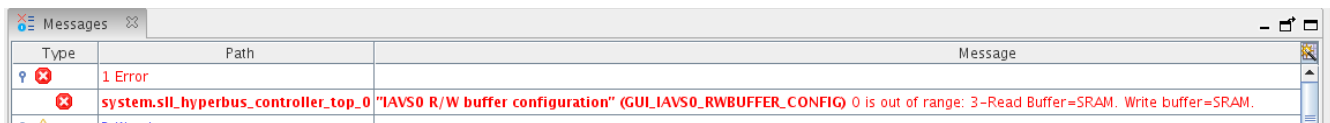
2. Synaptic Labs offers two Installation Guides that:
  - a. Begin by preparing you to enroll to receive a Full Featured Trial Edition license
  - b. Guide you on how to install the license file you will receive after enrolment
  - c. Guide you on how to install the Qsys components that you will receive after enrollment
3. Please download and read one of those Installation Guides:
  - a. Developers familiar with installing third party IP into Quartus will probably prefer the streamlined:  
[HBMC IP Installation Guide for Experience Developers.](#)
  - b. All other developers should download the:  
[HBMC IP Installation Guide with Detailed Step-by-Step Instructions.](#)

### Step 3: Install HBMC Qsys Component into the project IP Folder

1. In this tutorial we assume that S/Labs HyperBus Memory Controller (HBMC) will be located in the Project directory.
  - a. Other Qsys component installation methods are described in the above mentioned installation Guides.
2. Contact Synaptic Labs' for the latest version of Synaptic Labs' HBMC Full Featured edition IP
3. Copy S/Labs' HBMC Full Featured edition IP into the **project/ip** folder or IP installation folder.

### Step 4: Open Qsys and update S/Labs' HBMC configuration

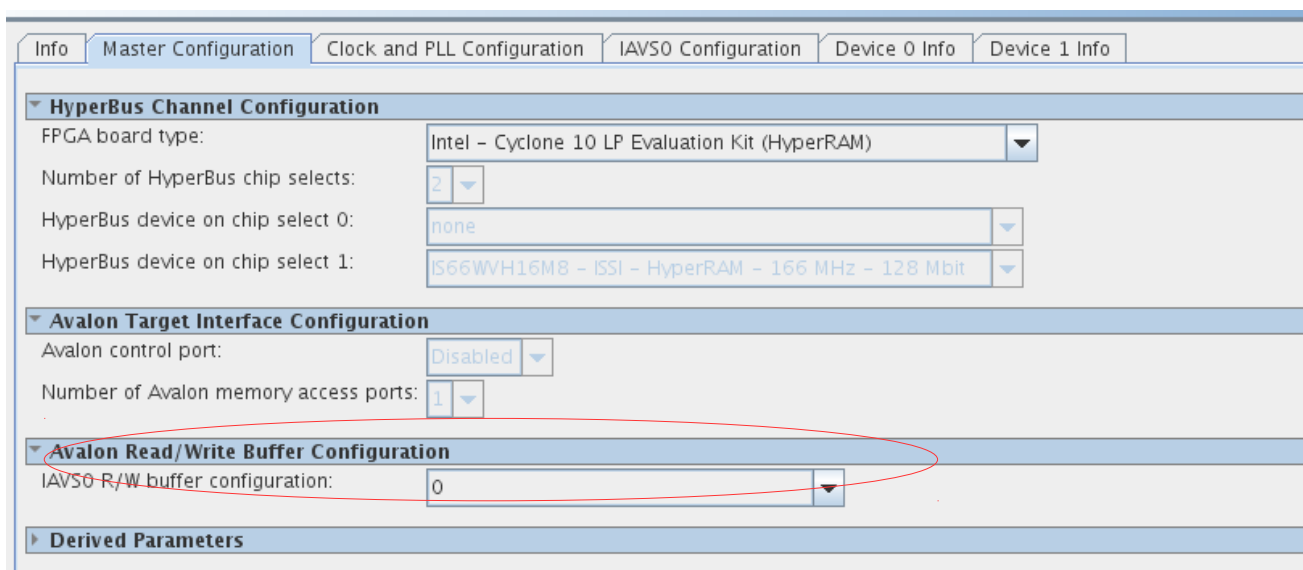
Ignore any errors and warning related to S/Labs' HBMC IP.



Double Click on S/Labs HBMC module

In the Master configuration Tab, change

- IAVS R/W buffer configuration to **Read Buffer=SRAM, Write Buffer = SRAM**



▼ Avalon Read/Write Buffer Configuration	
IAVS0 R/W buffer configuration:	Read Buffer=SRAM. Write buffer=SRAM. ▼

In the Clock and PLL configuratio Tab, change

- The **Avalon and HyperBus clock configuration** field is set to **Two clocks**
- The **HyperBus channel clock frequency** field is set to **150 MHz**
- The **Shared Avalon clock frequency** field is set to **100 MHz**

Info	Master Configuration	Clock and PLL Configuration	IAVS0 Configuration	Device 0 Info	Device 1 Info
▼ Clock Configuration					
Input clock (in_clk) frequency:		50	MHz		
Avalon and HyperBus clock configuration:		Two clocks–One clock for all the Avalon ports. One clock for the HyperBus channel ▼			
HyperBus channel clock frequency:		150 ▼	MHz		
Shared Avalon clock frequency:		100 ▼	MHz		
▼ Selected Configuration – Clocks					
Input clock (in_clk) frequency:		50	MHz		
HyperBus channel clock frequency:		150	MHz		
Avalon output clock (av_out_clk) frequency:		100	MHz		
Avalon IAVS0 port clock frequency:		100	MHz		
Avalon IAVS0 port clock crossing:		Low-area high-performance clock-crossing logic enabled			

The Hyperbus memory devices are now running at a higher frequency and offers higher throughput.

## Step 5: Follow the original tutorial

Please follow the original tutorials in order to generate the FPGA bitstream and software firmware.